Priyanjana Pal

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Google Scholar Profile

Experience

GlobalFoundries **Bangalore, India**
Senior Device-Circuit Co-Design and Enablement Engineer *Jan 2020–Nov 2022*

- **ESD Compact Modeling:** Measured and modeled the DC-IV, CV, TLP (HBM, CDM) characteristics of LV, MV, and HV ESD devices (e.g., LDMOS, VPNPs, BiSCR, Switch FETs) for nodes including 130nm, 45SPCLO, 28nm BCDlite, and 22FDX using SPECTRE and SPICE.
- **RF ESD Device and Circuit Design (with DE and US team):** Designed RF-compatible ESD designs for mmWave applications i.e., RF-diodes, ggNMOS, SCR-based clamps, and optimized performance using S-parameter model and EMX.
- **Model Automation and QA(with DE and US team):** Developed QA scripts (R and Python) for validating compact models, hardware correlation, and processing data across multiple technologies.
- **Layout Design and Tape-out:** Designed and taped out DC and RF test structures for compact modeling, including LVS/PEX extraction for BEOL resistance and capacitance using EMX and RF (S-parameter) modeling.
- **Collaboration and Training:** Trained peers in compact modeling workflows, including spectre simulations, layout design, and EMX/PEX extraction.

Education

Karlsruhe Institute of Technology (KIT) **Karlsruhe, Germany**
PhD in "Reliable Analog Computing" at CDNC, ITEC - Department of Computer Science *Dec 2022–Present*
Research in analog circuit design, reliability testing, and ML-trained neuromorphic circuits with **Prof. Mehdi Tahoori**, IEEE Fellow

Indian Institute of Technology (IIT) Gandhinagar **Gujarat, India**
M.Tech in Microelectronics and VLSI *2018–2020*
CGPA: 7.79/10. Thesis: Design and optimization of high voltage (HV) De-FinFETs for analog SoC using 3D-TCAD.

National Institute of Technology (NIT) Agartala **Agartala, India**
B.Tech in Electronics and Communication Engineering *2014–2018*
CGPA: 8.98/10

Research Interests

Analog and mixed-signal circuit co-design, neuromorphic computing, energy-efficient reliable circuit design, and machine learning integration in hardware.

Technical Skills

CAD Tools: Cadence Virtuoso, Synopsys DC, Sentaurus 3D TCAD, EMX, Calibre, QRC/XRC, PEX

Programming: Verilog, Verilog-A, Tcl, Linux scripting, R, Python

Languages: English (Fluent), Hindi (Fluent), Bengali (Native), German (A1 Level)

Design Projects

Three-Stage OTA for temperature stable classifer circuits:
- Achieved stable gain ($\approx 0.9\,\mathrm{V/V}$) and output current ($\approx 10.6\,\mu\mathrm{A}$) across $-20^{\circ}\mathrm{C}$ to $185^{\circ}\mathrm{C}$.
- Ensured robust PVT tolerance and stable reference voltage (0.5–$0.8\,\mathrm{V}$ at $V_{\mathrm{DD}} = 1$–$3\,\mathrm{V}$).

FlexIC Low Dropout Regulator:
- Designed a flexible LDO regulator with stable output voltage under wide PVT and thermal variations.
- Integrated structural delay-based Built-In Self-Test (BIST) techniques to ensure reliable operation in flexible substrates.

Low Dropout Regulator (LDO) in CMOS:
- Designed an LDO regulator in SCL 180 nm CMOS technology for digital applications.
- Achieved 200 mV dropout voltage with input voltage range of 2.0 V to 1.8 V.
- Specifications: Settling time of 200 ns, quiescent current of 10 μA, and PSRR of -40 dB at 1 MHz.

Bandgap Reference Circuit (BGR):
- Developed a low-power BGR circuit in SCL 180 nm technology for use in linear regulators.
- Achieved stable operation across 1.8–$2.5\,\mathrm{V}$ supply voltage and $-40^{\circ}\mathrm{C}$ to $125^{\circ}\mathrm{C}$ temperature, with only 50 μW power.

Temperature-Compensated Voltage Reference:
- Designed a CTAT–PTAT combined V_{ref} circuit to stabilize analog computing circuits under thermal variations.
- Achieved robust reference voltage (0.5–$0.8\,\mathrm{V}$) stability across $V_{\mathrm{DD}} = 1$–$3\,\mathrm{V}$ and wide temperature ($-20^{\circ}\mathrm{C}$ to $185^{\circ}\mathrm{C}$).
- Utilized stacked-NMOS and diode-connected transistor structures for balancing CTAT and PTAT responses, enhancing reliability of neuromorphic activations.

Binary Search ADC:
- Proposed a pruned binary-search ADC design optimized for flexible/printed electronics.

- Reduced area by $\sim 2\times$ compared to state-of-the-art printed ADCs and $\sim 5.4\times$ compared to flash ADCs.

CIM Resistive Memory Testing:
- Developed a trim-circuitry-based dynamic testing scheme for CIM (Compute-in-Memory) resistive memories.
- Enabled faster testing while maintaining high defect coverage.

Classifiers Design:
- **p-AMLP:** Implemented in Cadence Virtuoso at transistor level, realizing analog neurons and synapses with compact designs optimized for flexible substrates. Evaluated resilience and sensitivity trade-offs under PVT and fault injections.
- **p-DMLP:** Developed in RTL, with optimized arithmetic and multipliers for low-power printed electronics. Characterized vulnerability to digital faults and compared against analog counterpart.

Conference and Journal Publications

ICCAD 2025: SpikeSynth: Energy-Efficient Adaptive Analog Printed Spiking Neural Networks

ESWEEK 2025: PRINT-SAFE: PRINTed ultra-low-cost electronic X-Design with Scalable Adaptive Fault Endurance

DAC 2025: Power-Constrained Printed Neuromorphic Hardware Training

ICCAD 2024: Neural Architecture Search for Highly Bespoke Robust Printed Neuromorphic Circuits.

DATE 2024: Analog Printed Spiking Neuromorphic Circuit; On-Sensor Printed Machine Learning Classification via Bespoke ADC and Decision Tree Co-Design.

ETS 2024: Fault Sensitivity Analysis of Printed Bespoke Multilayer Perceptron Classifiers.

IEEE TCAD 2024: Neural Evolutionary Architecture Search for Compact Printed Analog Neuromorphic Circuits.

ICCAD 2023: Power-Aware Training for Energy-Efficient Printed Neuromorphic Circuits.

ASPDAC 2024: A Dynamic Testing Scheme for Resistive-Based Computation-In-Memory Architectures.

Teaching & Mentoring

Graduate Supervision (KIT, 2024–Present): Supervised master's theses on spiking neuromorphic circuits and computing systems, including STDP-based supervised learning and variation-aware design/testing.

PSE/TSE Project Supervision (2024–Present): Guided student projects such as a University Chatbot for automated Q&A and an LSTM-based music generation.

Labs (Analog & Reliability): Conducted hands-on chip-design labs with Cadence, and layout automation.

Leadership (PRICOM Project Proposal, 2022–2025): Collaborated with PragmatIC and IMEC for flexIC PDK access and layout automation; coordinated Horizon EU PRICOM project, including reporting and proposal contributions.

Achievements

Awards: Received multiple appreciation and spotlight awards at GlobalFoundries for ESD compact model development.

Scholarships: National Visual Arts Painting Scholarship by CCRT, India, North-Eastern-Council (NEC) Scholarship in Bachelor's, Early Admit MTech with MHRD, India, GATE'2018.

Hobbies

Activities: Painting, Swimming, Chess, Cooking

References

- **Prof. Mehdi B. Tahoori (Ph.D. Advisor)**, CDNC-KIT — mehdi.tahoori@kit.edu
- **Dr. Dattatreya Prabhu Rachakonda**, ESD Manager, GF, India — dattatreyaprabhu.rachakonda@globalfoundries.com
- **Mr. Rakesh Kumar Pothal**, Staff Design Engineer, Semtech, India — rpothal@semtech.com
- **Dr. Sani R. Nassif**, Visiting Professor at KIT, CEO of Radyalis, Austin, TX USA — srn@radyalis.com
- **Dr. Anindya Nath**, Staff Design Engineer, IBM Research, Albany, NY, USA — anindya.nath@gmail.com

Additional references available upon request.